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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/509,220	09/24/2004	Colin King	GB02 0032 US	5146

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EXAMINER	
TSAI, SHENG JEN	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 12/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/509,220	KING, COLIN	
	Examiner	Art Unit	
	Sheng-Jen Tsai	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-11 are presented for examination in this application (10,509,220) filed on September 24, 2004.

2. ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-6 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Chauvel et al. (US 6,606,687).

As to claim 1, Chauvel et al. disclose **a method of context switching between processes in a computer operating system including writing cached data back to a memory means** [Optimized Hardware Cleaning Function foe VIVT Data Cache (title); Accordingly, as part of the context switch between tasks, the operating system must invalidate the content of the cache so that the cache values are consistent with the main memory for each task (column 4, lines 18-22)], **comprising the step of the writing cached data back to the memory means during processor idle cycles at completion of a process and prior to initiation of the context switch** [Cleaning a cache requires that all locations marked as dirty must be written back to the main memory 16 (column 4, lines 44-45); During a context switch, or at other times where a

cache clean is necessary, software initiates a hardware clean function in block 50 (column 5, lines 63-65); As will be described in greater below, the hardware cleaning routine is interruptible and will return control to the software if there is an interrupt or if the clean operation is complete (column 5, lines 66-67 and column 6, lines 1-2)].

As to claim 2, Chauvel et al. teach that **a method as claimed in claim 1, including the step of setting a flag to indicate cached data has been written back to memory subsequent to the completion of the process** [The cache controller sets a flag (a "dirty bit") along with the tag at location N2 to indicate that this cache location is not consistent with the main memory 16. This is often referred to as a dirty cache location (indicated by a "D" in the tag memory 20 of FIG. 2) (column 4, lines 39-42); If the dirty bit is set in decision block 42, then the corresponding information in data array 20 at location n is copied to main memory at the physical address corresponding to the virtual address stored in tag memory 22 at location n. Thus, for location n=N2, since the dirty bit is set, the data in data memory 22 at location N2 would be written to physical address PA1. After the entry is saved to main memory 16, or if the dirty bit was not set in decision block 42, the clean function is complete in block 46 and control returns to the software routine (column 5, lines 11-20)].

As to claim 3, Chauvel et al. teach that **a method as claimed in claim 2, including the step of, at the time of requiring a context switch, checking for the said flag to identify if the previous process's cached data has been written back to memory** [The cache controller sets a flag (a "dirty bit") along with the tag at location N2 to indicate that this cache location is not consistent with the main memory 16. This

is often referred to as a dirty cache location (indicated by a "D" in the tag memory 20 of FIG. 2) (column 4, lines 39-42); If the dirty bit is set in decision block 42, then the corresponding information in data array 20 at location n is copied to main memory at the physical address corresponding to the virtual address stored in tag memory 22 at location n. Thus, for location n=N2, since the dirty bit is set, the data in data memory 22 at location N2 would be written to physical address PA1. After the entry is saved to main memory 16, or if the dirty bit was not set in decision block 42, the clean function is complete in block 46 and control returns to the software routine (column 5, lines 11-20)].

As to claim 4, Chauvel et al. teach that **a method as claimed in claim 3, including the step of, upon identifying that the said flag has been set, conducting the context switch without further cache write-back to memory** [Write-back (or "copy back) caches reduce power consumption and increase speed by writing only to the cache 18 until an event occurs which requires updating the main memory 16 (column 4, lines 25-28); Cleaning a cache requires that all locations marked as dirty must be written back to the main memory 16 (column 4, lines 44-45)].

As to claim 5, Chauvel et al. disclose **a method as claimed in claim 3, and including the step of conducting a cached data write-back to memory at the time of requiring a context switch if the said flag has not been identified as set** [Cleaning a cache requires that all locations marked as dirty must be written back to the main memory 16 (column 4, lines 44-45)].

As to claim 6, refer to "As to claim 1."

As to claim 11, refer to "As to claim 1."

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chauvel et al. (US 6,606,687), and in view of Pawlowski et al. (US 5,537,640).

As to claim 7, Chauvel et al. do not explicitly mention that **a system as claimed in claim 6, and arranged to employ a processor sleep mode to write cache data back to memory automatically during a sleep period**.

However, Pawlowski et al. disclose in their invention "Asynchronous Modular Bus Architecture with Cache Consistency" a method of performing cache write back automatically during a sleep period [In some embodiments, write-backs take place at predetermined intervals such as during CPU idle times (column 17, lines 10-11)].

Performing cache write back automatically during a sleep period makes best utilization of CPU's capacity, hence enhancing the system throughput.

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicant's invention to recognize of performing cache write back automatically during a sleep period, as demonstrated by Pawlowski et al., and to incorporate it into

the existing system disclosed by Chauvel et al. to further enhance the throughput of the system.

As to claim 8, Pawlowski et al. teach that **a system as claimed in claim 6, and including a status register having a flag for initiating data cache write-back during a CPU sleep operation** [In some embodiments, write-backs take place at predetermined intervals such as during CPU idle times (column 17, lines 10-11); MODIFIED* MODIFIED* is the snoop status signal available with respect to the activation of SPRDY*. When active, it indicates that the CPU module must perform a write-back cycle to memory. If inactive, the CPU module does not need to perform a write-back cycle (column 7, lines 31-35)].

As to claim 9, Pawlowski et al. teach that **a system as claimed in claim 6, wherein the operating system is arranged with an additional sleep code instruction for the data cache write-back** [In some embodiments, write-backs take place at predetermined intervals such as during CPU idle times (column 17, lines 10-11); column 20, lines 13-45].

As to claim 10, Pawlowski et al. teach that **a system as claimed in claim 9, wherein the sleep code of the processor includes an additional data cache write-back instruction** [In some embodiments, write-backs take place at predetermined intervals such as during CPU idle times (column 17, lines 10-11); column 20, lines 13-45].

6. ***Related Prior Art***

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Prabhu, (US Patent Application Publication 2003/0056062), "Preemptive Write Back Controller."
- Chauvel et al., (US 6,321,299), "Computer Circuits, Systems, and Methods Using Partial cache Cleaning."

Conclusion

7. Claims 1-11 are rejected as explained above.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sheng-Jen Tsai
Examiner
Art Unit 2186

November 1, 2006

PIERRE BATAILLE
PRIMARY EXAMINER
11/29/06